域格信息技术有限公司
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# CLM920_TE3 hardware user guide

## Version 1.4



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# Document history

## Revision record

| Version | Date | Description | Author |
|---|---|---|---|
| V1.0 | 20160812 | Initial | David |
| V1.1 | 2017/6/30 | Add CLM920 TE3 | |
| V1.2 | 2017/9/13 | Correct errors | |
| V1.3 | 2017/11/2 | Correct errors | |
| V1.4 | 2017/11/8 | Add Band | |
| | | | |
| | | | |
| | | | |

# List

# 1 Introduction

This document is a wireless solution product, CLM920_TE3, 4G module hardware interface manual, describes the hardware composition and function features of the module and application interface definition and usage instructions also Electrical & mechanical characteristics, etc. which provide hardware description for user's application development based on this product.

## Term and abbreviation

| | | |
|---|---|---|
| ADC | Analog-Digital Converter | etc |
| AFC | Automatic Frequency Control | |
| AGC | Automatic Gain Control | |
| ARFCN | Absolute Radio Frequency Channel Number | |
| B2B | Board to Board Connector | |
| BER | Bit Error Rate | |
| CDMA | Code Division Multiple Access | |
| DAI | Digital Audio interface | |
| DAC | Digital-to-Analog Converter | |
| DSP | Digital Signal Processor | |
| DTR | Data Terminal Ready | |
| EFR | Enhanced Full Rate | |
| EMC | Electromagnetic Compatibility | |
| EMI | Electro Magnetic Interference | |
| ESD | Electronic Static Discharge | |
| EVDO | Evolution Data Only | |
| FR | Full Rate | |
| GPRS | General Packet Radio Service | |
| HR | Half Rate | |
| IMEI | International Mobile Equipment Identity | |
| ISO | International Standards Organization | |
| PLL | Phase Locked Loop | |
| PPP | Point-to-point protocol | |
| RAM | Random Access Memory | |
| ROM | Read-only Memory | |
| RTC | Real Time Clock | |
| SMS | Short Message Service | |

| | | |
|---|---|---|
| UART | Universal asynchronous receiver-transmitter | |
| UIM | User Identifier Management | |
| USB | Universal Serial Bus | |
| VSWR | Voltage Standing Wave Ratio | |

# 2 Product summary

## 2.1 Product brief

CLM920_TE3 Module baseband chip using Qualcomm MDM9X07,it is integrate FDD/TDD/TD-SCDMA/UMTS/EVDO/CDMA/EDGE/GSM support multiple network formats and GPS,supported OS: Windows7/Windows8/Windows10/Android4.0 embedded operating system. CLM920_TE3 4G Module can be applied to the following applications：

- ✧ Vehicle equipment
- ✧ Wireless POS terminal
- ✧ Wireless advertising, media
- ✧ Remote monitoring system
- ✧ An intelligent meter reading
- ✧ Mobile broadband internet service
- ✧ Other wireless terminals

## 2.2 Module characteristics

Figure 2-1 CLM920_TE3

| Name | Description |
|---|---|
| CLM920_TE3 | LTE for CMCC,CUCC and CTCC, support SRLTE,GPS and Analog audio |
| CLM920_TB3 | LTE for CMCC and CUCC, support SRLTE,GPS and Analog audio |

Figure 2-2 CLM920_TE3 4G key characteristics

| Characteristics | Description |
|---|---|
| size | 32mmx29mmx2.4mm |
| Soldering Type | LCC |
| Application processor | ARM Cortex-A7,1.2GHz,256kB |
| Supported band (CLM920_NC3) | ✧ LTE（FDD）B1/B3/B5/B8<br>✧ LTE (TDD) B38/B39/B40/B41<br>✧ UMTS/HSDPA/HSUPA Band B1/B5/B8<br>✧ TD-SCDMA B34/B39<br>✧ GSM/GPRS/EDGE Tri Band 850/900/1800<br>✧ CDMA2000 1X/EVDO BC0 |

| | |
|---|---|
| Supported band (CLM920_TB3) | ✧ LTE（FDD）B1/B3/B5/B8<br>✧ LTE (TDD) B38/B39/B40/B41<br>✧ UMTS/HSDPA/HSUPA Band B1/B5/B8<br>✧ TD-SCDMA B34/B39<br>✧ GSM/GPRS/EDGE Tri Band 900/1800 |
| Supported band（CLM920_TE3） | ✧ LTE (FDD)B1/B3/B5/B7/B8/B20<br>✧ LTE (TDD) B38/B39/B40/B41<br>✧ WCDMA B1/B5/B8<br>✧ TD-SCDMA B34/B39<br>✧ GSM/GPRS/EDGE Tri Band 850/900/1800 |
| Working Voltage | 3.3V—4.2V, Typical type 3.7V |
| working temperature | Normal: –30°C to +75°C<br>Extreme: –40°C to +85°C<br>Storage： -45°C to +90°C |
| Interface | Standard USIM,supported 3.0V/1.8V, hot swap function |
| | USB2.0 (High-Speed) |
| | Hardware reset |
| | UART |
| | PCM |
| | SD card |
| | SPI |
| | Power supply |
| | LEDs for status |
| | GPIOs |
| Antenna | Main Antenna（Pin49） |
| | Diversity Antenna（Pin35） |
| | GPS Antenna（Pin47） |
| TX power | Class 4 (33dBm±2dB) for GSM900 |
| | Class 1 (30dBm±2dB) for DCS1800 |
| | Class E2 (27dBm±3dB) for GSM900 8-PSK |
| | Class E2 (26dBm±3dB) for DCS1800 8-PSK |
| | Class 3 (24dBm±1dB) for CDMA BC0 |
| | Class 3 (24dBm+1/-3dB) for WCDMA bands |
| | Class 3 (24dBm+1/-3dB) for TD-SCDMA bands |
| | Class 3 (23dBm±2dB) for LTE FDD bands |
| | Class 3 (23dBm±2dB) for LTE TDD bands |
| | GPRS: Class12 DL 85.6 kbps/UL 85.6 kbps |
| | EDGE: Class12 DL 236.8 kbps/UL 236.8 kbps |
| | WCDMA CS: DL 64 kbps/UL 64 kbps |
| | WCDMA PS: DL 384 kbps/UL 384 kbps |
| | TDD-HSPA: DL 2.8Mbps/UL 2.2Mbps |

| | |
|---|---|
| Uplink/Downlink Speed | TDD-HSPA+: Relese3 DL 4.2Mbps/UL 2.2Mbps |
| | HSPA+: DL 21.6 Mbps/UL 5.76 Mbps |
| | DC-HSPA+:R8 DL 42 Mbps/UL 5.76 Mbps |
| | CDMA 1X: DL 153.6kbps/UL 153.6kbps |
| | CDMA 1xEVDOr0: DL 2.4Mbps/UL 153kbps |
| | CDMA 1xEVDOrA: DL 3.1Mbps/UL 1.8Mbps |
| | LTE FDD:DL 150Mbps/UL 50Mbps@20M BW cat4 |
| | LTE TDD:DL 130Mbps/UL 35Mbps@20M BW cat4 |
| Positioning system | GPS/BEIDOU/GLONASS |
| Diversity Antenna | LTE/WCDMA/TDSCDMA/EVDO |
| AT-command | Standard AT command（Hayes 3GPP TS 27.007 & 27.005） |
| Tethering | RNDIS for Windows |
| Humidity range | 5%～95% |
| Label Index | M:main antenna,D:diversity,G:GPS, V:voice<br>CLM_920_TE3 mdgv :supported "main Ant/div Ant/gps/voice" |

## 2.3 Module function

CLM920_TE3 4G module mainly contains the following circuit units：

- ✧ Baseband for RF
- ✧ Power management system
- ✧ NAND/DDR2
- ✧ Radio Frequency TX/RX
- ✧ RF front end
- ✧ GPS Receive
- ✧ I/O interface

CLM920_TE3 4G functional block diagram is shown below：

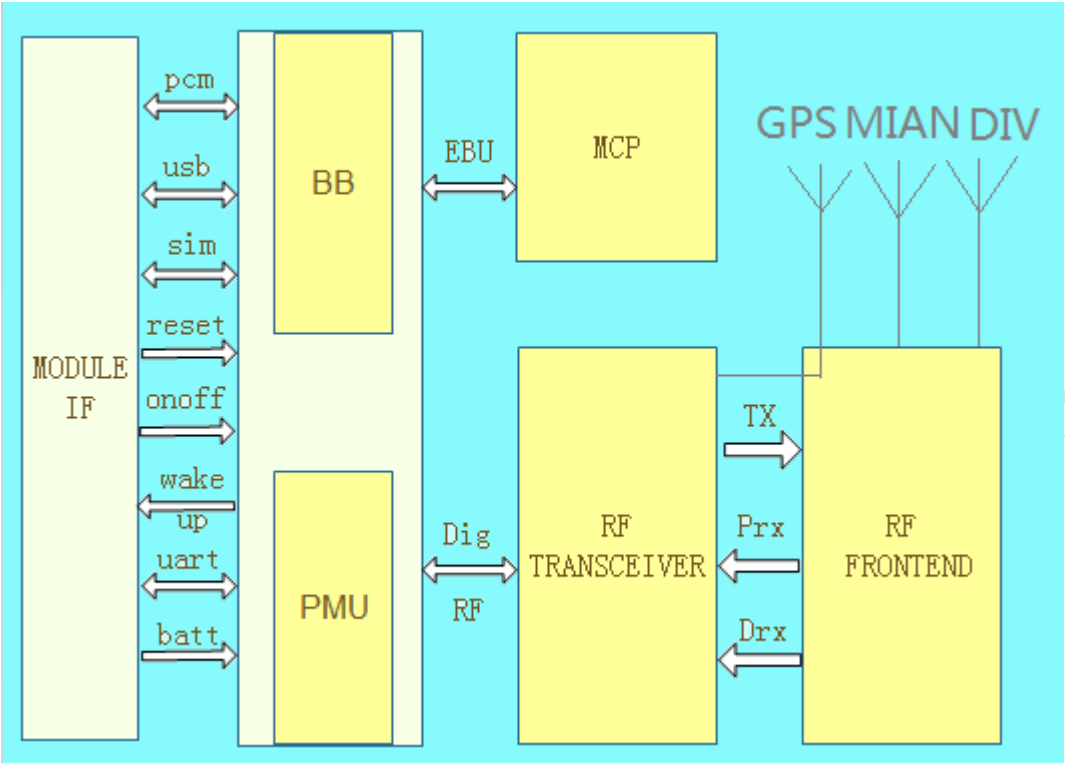



Figure **1 CLM920_TE3 4G Block diagram**

# 3 Interface description

## 3.1 Description

- ✧ I/O definition
- ✧ Power supply interface
- ✧ USB interface
- ✧ UART interface
- ✧ USIM interface
- ✧ SD interface
- ✧ SPI interface
- ✧ Airplane mode interface
- ✧ GPIO interface
- ✧ LED status interface
- ✧ Antenna interface
- ✧ Voice interface

## 3.2 Module interface

### 3.2.1 I/O definition

Figure 3-1：Parameter definition

| Type | Description |
|---|---|
| DO | Data Out |
| IO | IN/Out |
| DI | Data In |
| AO | Analog Out |
| OD | Open Drain |
| PI | Power IN |
| PO | Power Out |
| AI | Analog In |

CLM920_TE3 4G module interface definition is shown in the following table：

Figure 3-2 interface definition

| PIN | PIN Name | I/O | Description | Mark |
|---|---|---|---|---|
| 1 | WAKEUP_IN | DI | Sleep mode control | Open, if it is not used |
| 2 | AP_READY | DI | Sleep state detection | Open, if it is not used |
| 3 | RESERVED | | Reserved | Open |
| 4 | W_DISABLE | DI | Flight mode control | Open, if it is not used |
| 5 | NET_MODE | DO | Indicate network status | Open, if it is not used |
| 6 | NET_STATUS | DO | Indicate network status | Open, if it is not used |
| 7 | VREG_1.8V | PO | Output1.8V | Max 50mA current |
| 8 | GND | | Ground | |
| 9 | GND | | Ground | |
| 10 | GND | | Ground | |
| 11 | DBG_RX | DI | UART RX | Open, if it is not used |
| 12 | DBG_TX | DO | UART TX | Open, if it is not used |
| 13 | SIM_DET | DI | USIM detect | Open, if it is not used |
| 14 | USIM_VCC | PO | USIM power supply | |
| 15 | USIM_DATA | IO | USIM DATA | |
| 16 | USIM_CLK | DO | USIM clock | |
| 17 | USIM_RST | DO | USIM reset | |
| 18 | RESERVED | | Reserved | Open |
| 19 | GND | | Ground | |
| 20 | RESET_N | DI | Reset | Active LOW |

| | | | | |
|---|---|---|---|---|
| 21 | ON/OFF | DI | Power ON/OFF | Active LOW |
| 22 | GND | | Ground | |
| 23 | VREG_2.85V | PO | Output 2.85V for SD-card | Max 50mA |
| 24 | PCM_IN | DI | PCM Data In | Open, if not used |
| 25 | PCM_OUT | DO | PCM Data Out | Open, if not used |
| 26 | PCM_SYNC | IO | PCM Sync | Open, if not used |
| 27 | PCM_CLK | IO | PCM clock | Open, if not used |
| 28 | SD_D3 | IO | SDIO Data | Open, if not used |
| 29 | SD_CLK | DO | SDIO clock | Open, if not used |
| 30 | SD_CMD | IO | SDIO command | Open, if not used |
| 31 | SD_D1 | IO | SDIO Data | Open, if not used |
| 32 | SD_D2 | IO | SDIO Data | Open, if not used |
| 33 | SD_D0 | IO | SDIO Data | Open, if not used |
| 34 | SD_INT | IO | SDIO detect | Open, if not used |
| 35 | ANT_DRX | AI | Diversity | 50ohm impedance |
| 36 | GND | | Ground | |
| 37 | SPI_MISO | DI | SPI In | Open, if not used |
| 38 | SPI_CS | DO | SPI Chip Select | Open, if not used |
| 39 | SPI_CLK | DO | SPI Clock | Open, if not used |
| 40 | SPI_MOSI | DO | SPI Out | Open, if not used |
| 41 | I2C_SCL | OD | I2C Clock | Open, if not used |
| 42 | I2C_SDA | OD | I2C Data | Open, if not used |
| 43 | RESERVED | | Reserved | Open, if not used |
| 44 | ADC1 | AI | A/D converter | Open, if not used |
| 45 | ADC0 | AI | A/D converter | Open, if not used |
| 46 | GND | | Ground | |
| 47 | ANT_GNSS | AI | GNSS Antenna | 50ohm impedance |
| 48 | GND | | Ground | |
| 49 | ANT_MAIN | IO | Main Antenna | 50ohm impedance |
| 50 | GND | | Ground | |
| 51 | GND | | Ground | |
| 52 | GND | | Ground | |
| 53 | GND | | Ground | |
| 54 | GND | | Ground | |
| 55 | MCLK | DO | I2S Clock | Open, if not used |
| 56 | GND | | Ground | |
| 57 | VBAT | PI | Main Power supply In | |

| | | | | |
|---|---|---|---|---|
| 58 | VBAT | PI | | Current reached to 2A |
| 59 | VBAT | PI | | |
| 60 | VBAT | PI | | |
| 61 | STATUS | OD | LED indication | Open, if not used |
| 62 | RI | DO | RING indication/Wakeup | Open, if not used |
| 63 | DCD | DO | UART Carrier Detect | Open, if not used |
| 64 | UART_CTS | DO | UART CTS | Open, if not used |
| 65 | UART_RTS | DI | UART RTS | Open, if not used |
| 66 | UART_DTR | DI | UART DTR | Open, if not used |
| 67 | UART_TXD | DO | UART TX | Open, if not used |
| 68 | UART_RXD | DI | UART RX | Open, if not used |
| 69 | USB_DP | IO | USB + | 90 ohm impedance |
| 70 | USB_DM | IO | USB - | 90 ohm impedance |
| 71 | USB_VBUS | PI | USB VBUS | 5V input |
| 72 | GND | | Ground | |
| 73-84 | RESERVED | | Reserved | Open, if not used |
| 85-112 | GND | | Ground | |
| 113-116 | RESERVED | | Reserved | Open, if not used |
| 117-140 | RESERVED | | Reserved | Open, if not used |
| 141-144 | RESERVED | | Reserved | Open, if not used |

### 3.2.2 PIN allocation

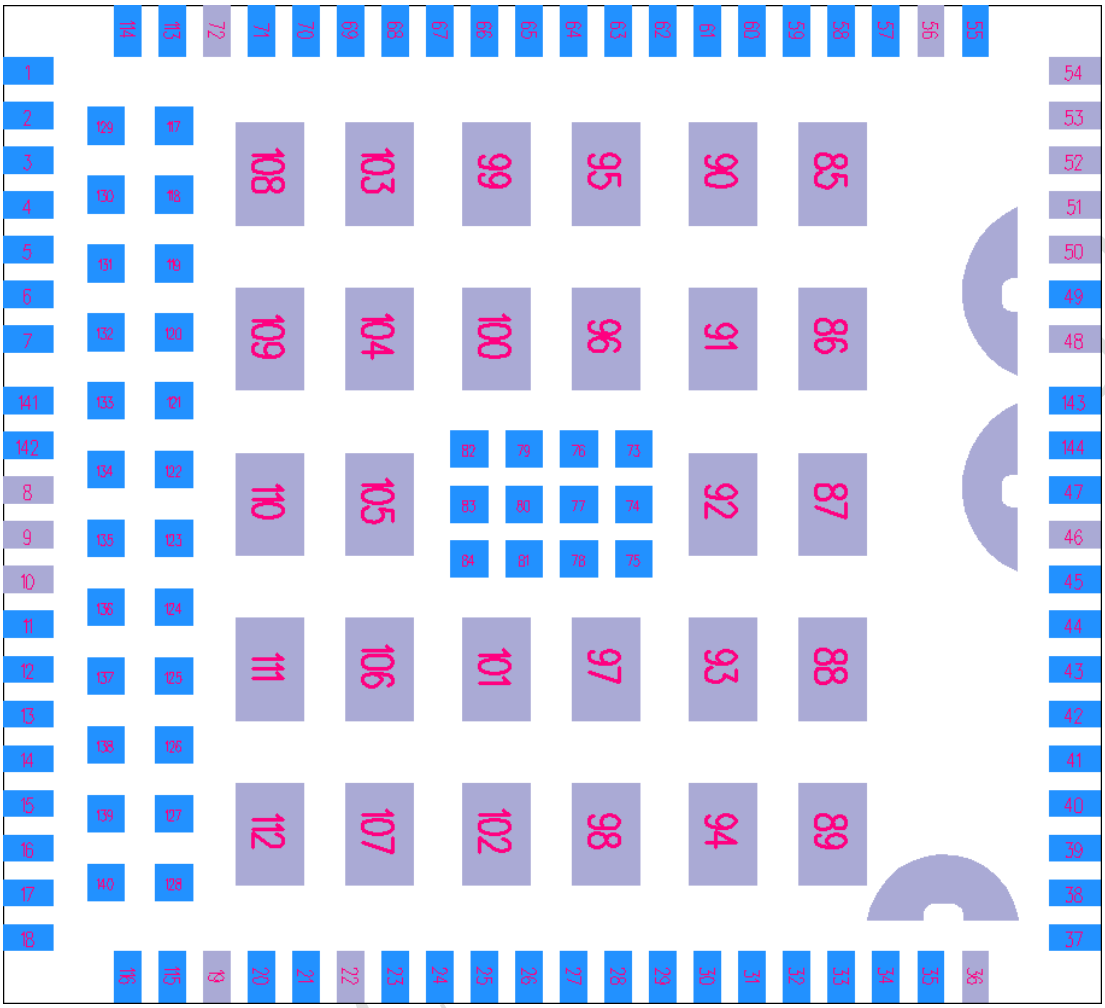



Figure **2** **CLM920_TE3 PIN allocation**

## 3.3 Power Supply

### 3.3.1 interface introduction

CLM920_NC5 4G module power supply interface consist of four part：

- ✧ VBAT: main power supply(battery also can be used)
- ✧ VREG_USIM: USIM power supply
- ✧ VREG_1.8V: Output, max current 50mA
- ✧ VREG_2.85V: TF card power supply, max current50mA.

### 3.3.2 Power Supply design

CLM920_TE3 4G has four VBAT pins are used connect external power supplies, can be divided into two power domain, one is(59,60pin)used baseband chipset, the other is (57,58pin)used RF power supplies, range is 3.3V~4.2V, we are recommend to use 3.3V/2A, Module can be generate a peak current of 2A at the instant of transmitting maximum rate. It might be bit ripples, so recommend to use one 150uF Cap and three 47uF Caps. The power line should not be less than the line 2mm. Recommend to use MOS control VBAT power supply, so that the module can be completely powered off, reference the following circuit design：

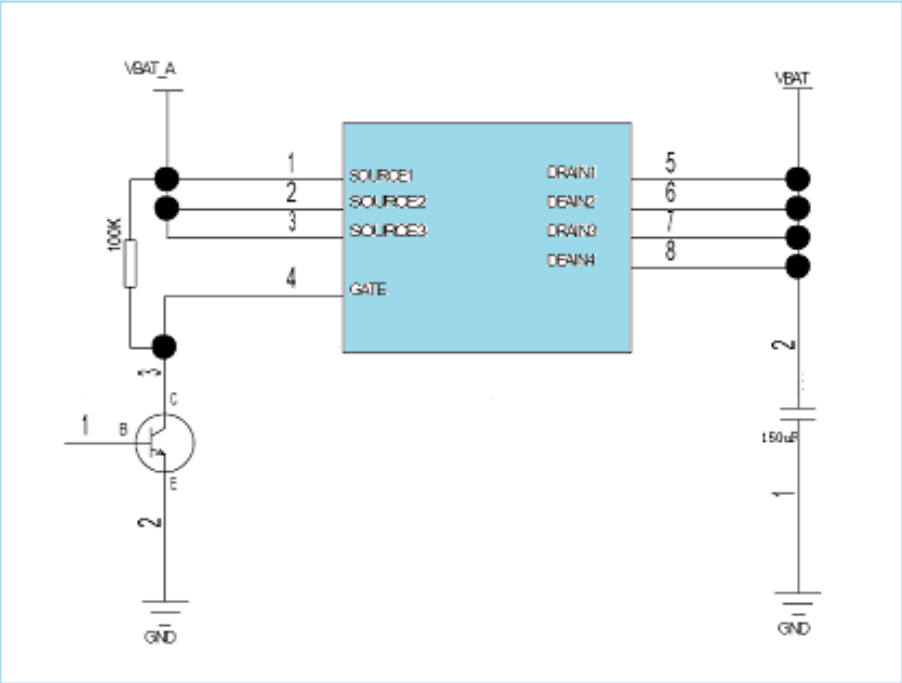



**Figure 3 Reference circuit of power supply**

CLM920_TE3 4G module power interface is as follows：

Figure 3-3 Definition of power supply pin

| PINs | Name | I/O | Description | Characters（V） | | |
|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX |
| 57,58,59,60 | Power | In | Main | 3.3V | 3.8V | 4.2V |
| 14 | SIM | Out | USIM | 0 | 1.8/2.85V | 1.98/3.3V |
| 7 | VREG_1.8 | Out | GPIO | 1.8V | 1.8V | 1.8V |
| 34 | VREG_2.85 | Out | TF | 1.8V | 2.85V | 2.95V |

## 3.4 Power ON/OFF

Power ON： Pull it LOW 2~3sec,when you need to Power ON.

Figure 3-4 Power ON/OFF PIN

| PIN | Name | Level | Description |
|---|---|---|---|
| 21 | PWRKEY | 1.3V-2.1V | Active LOW |

Power on time sequence diagram:

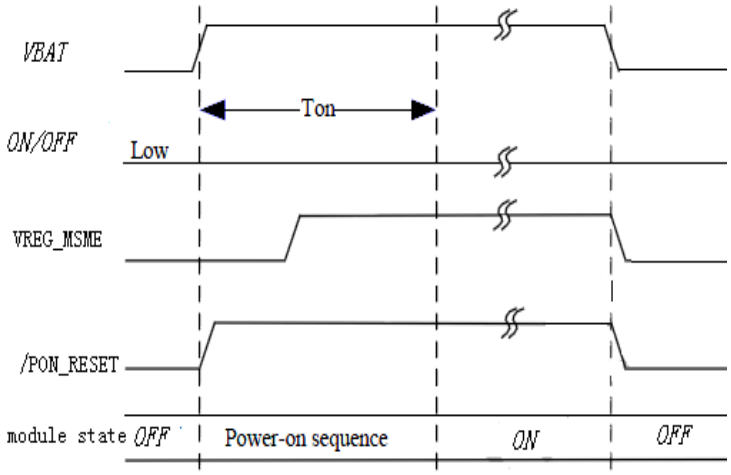



Figure **4** **Power ON sequence**

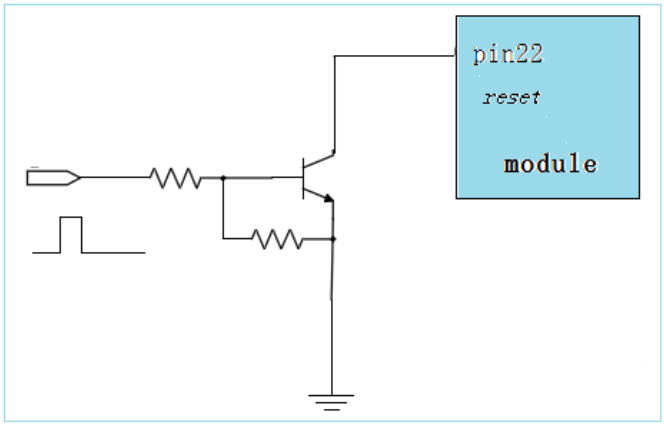



**图 5 Power ON Circuit**

Power OFF：In Power ON status, press PWRKEY(active LOW)and release it.

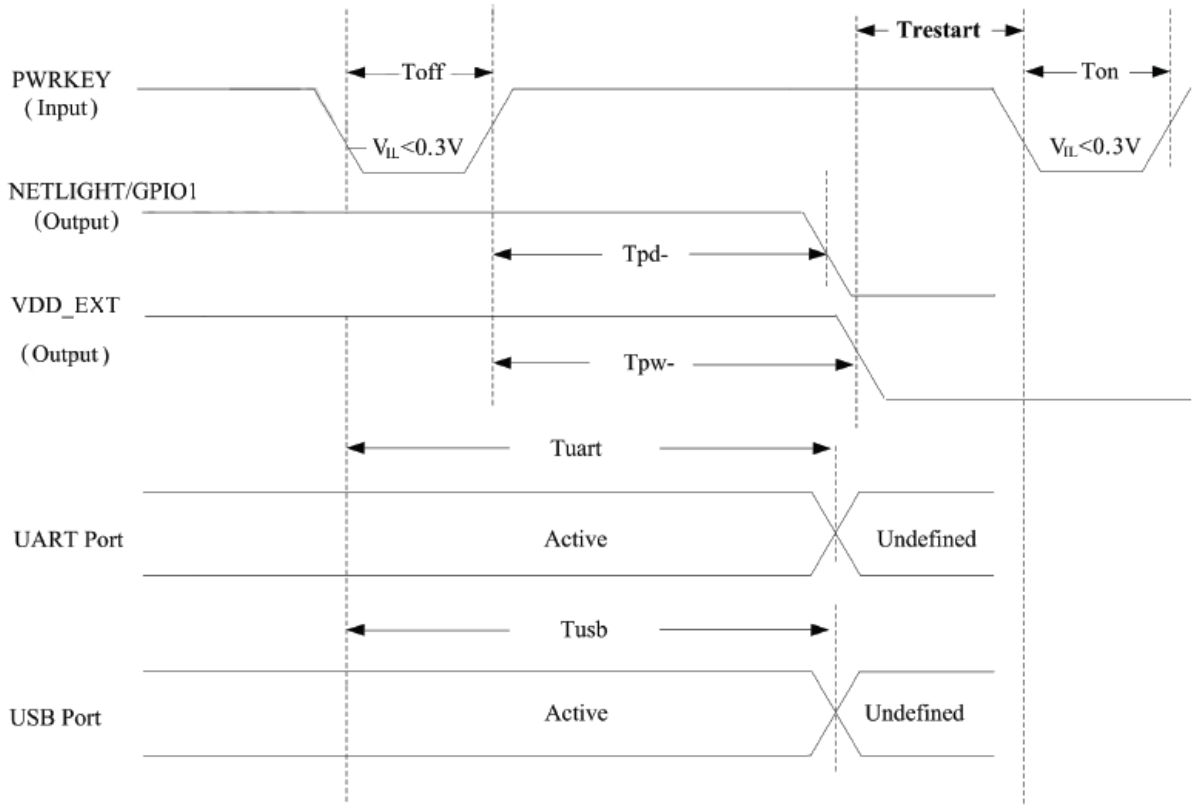



Figure 6 **Power OFF sequence**

## 3.5 Reset

RESET_N use for module reset. Pull RESET pin LOW(200ms above).

Figure 3-5 Reset PIN Definition

| PIN | Name | Level | Description |
|---|---|---|---|
| 20 | RESET | 1.3V-2.1V | Reset, Active LOW |

RESET：Pull this PIN LOW (200ms)module will be reset immediately, this pin need to pull-up resistor 10K is recommended at 1.8V. The pin is sensitive to the interference ratio and should be protected.

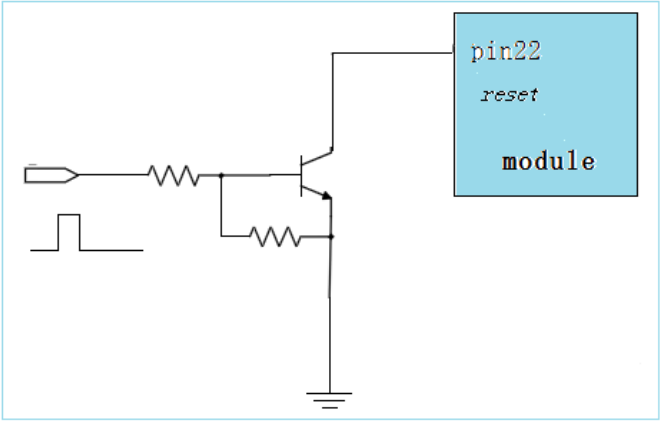



**Figure 7 Reset reference circuit**

## 3.6 USB Interface

CLM920_TE3 support USB2.0 high speed at (480Mbps), Full speed at（12Mbps）and follow USB2.0 characteristic.

USB PIN description：

Figure 3-6 USB Pin description

| PINs | Name | I/O | Description |
|---|---|---|---|
| 71 | USB_VBUS | PI | USB VBUS |
| 70 | USB_D- | IO | USB- |
| 69 | USB_D+ | IO | USB+ |

USB usage：

1: When the module go into sleep mode, DTR should be HIGH or OPEN. When the module went into sleep mode, sending data to the module by USB will wake up the module, and module has URC on time, the RI signal will wake up the host.

2：If the host doesn't support suspend mode, you can disconnect the USB_VBUS through the external control circuit so that the module goes into sleep mode, restoring USB_VBUS power supply can wake up the module.

USB reference circuit as below：

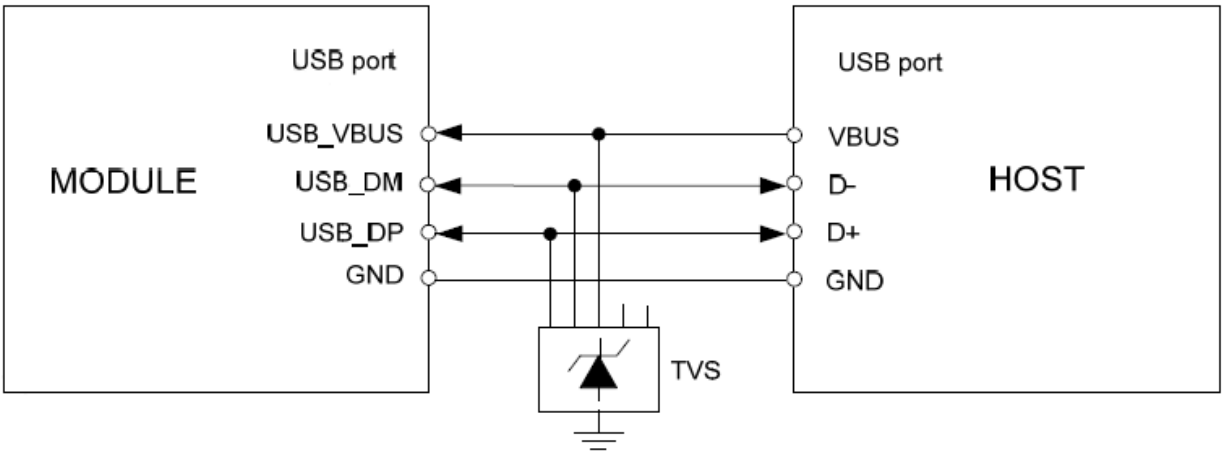



**Figure 8 USB reference circuit**

Design note：

1. USB routing design needs to strictly comply with the requirements of USB2.0 protocol, pay attention to the protection of the data line, differential line, control impedance is 90 ohm, the upper and lower left and right ground handling.
2. ESD protection should be added on the data line, the parasitic capacitance of the protection devices should not exceed 2pF, and the ESD devices should be placed as close as possible to the USB.
3. Modules can only serve as slave devices for USB buses.

USB interface can support the following functions：

- ✧ Software upgrade
- ✧ Data communication
- ✧ AT Command
- ✧ GNSS NMEA output

## 3.7 UART Interface

CLM920_TE3 provides two groups of UART interfaces: One group is the main serial port, voltage level is 1.8V, support 9600,19200,38400,57600,115200,230400,460800,921600bps baud rate, default value is 115200bps, serial port level is 1.8V.

Figure 3-7 UART pin description

| PIN | Name | I/O | Description |
|---|---|---|---|
| 62 | UART_RI | DO | Ring Indicator |
| 63 | UART_DCD | DO | DCD |
| 64 | UART_CTS | DO | CTS |
| 65 | UART_RTS | DI | RTS |
| 66 | UART_DTR | DI | DTR |

| | | | |
|---|---|---|---|
| 67 | UART_TXD | DO | TX |
| 68 | UART_RXD | DI | RX |

Serial port usage：

When the host and the module are connected through the serial port, Module can into sleep mode by pulling the DTR HIGH, pulling down the DTR to wake up the module, when URC report, RI signal will send a signal to wake up the host.

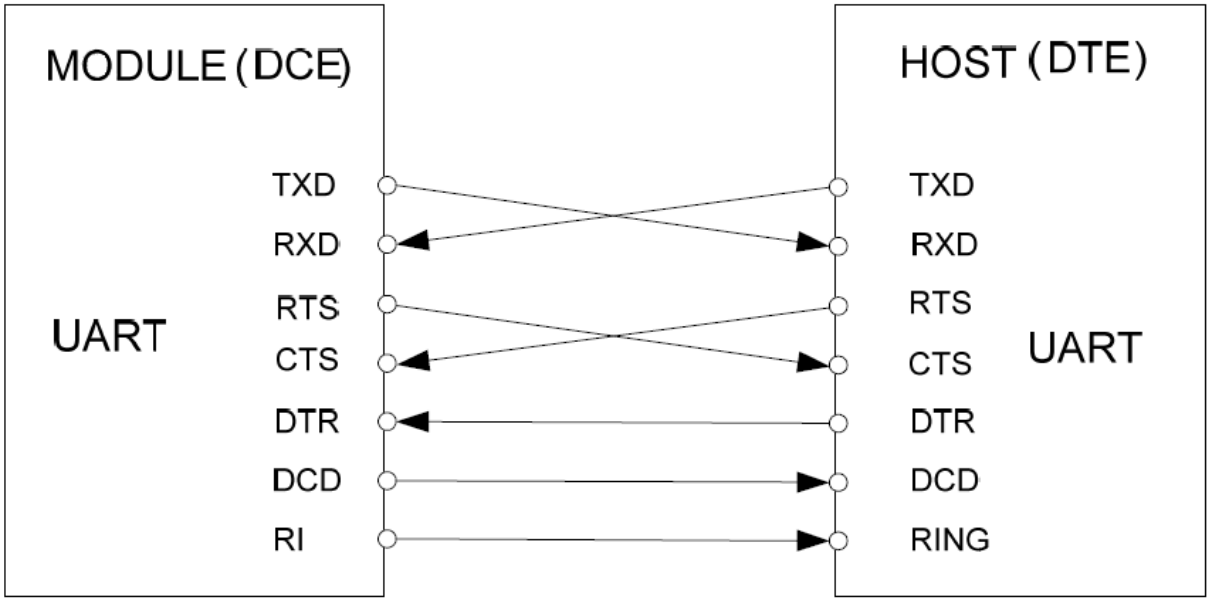



**Figure 9 UART Pins**

Debug UART：

Debugging serial port, default baud rate 115200bps, print log UART as below：

Figure 3-8 UART debugging pin

| PIN | Name | I/O | Description |
|---|---|---|---|
| 11 | DBG_RXD | DI | RX |
| 12 | DBG_TXD | DO | TX |

For a debug log print, reference below circuit

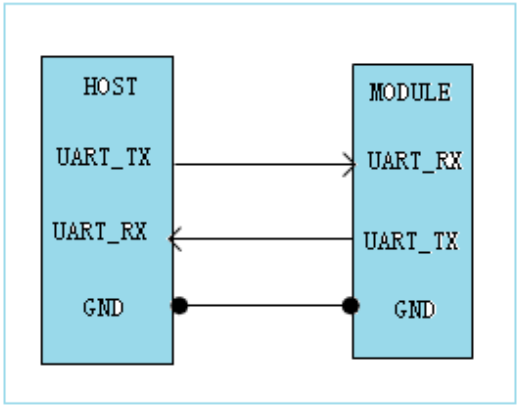


Figure **10 UART Debug Pin**

## 3.8 USIM Interface

CLM920_TE3 provides a USIM card interface compatible with ISO 7816-3 standard, and supports 1.8V/3.0V USIM card. The module automatically identifies 1.8V or 2.85V USIM card.

Figure 3-9 USIM PINs

| PINs | Name | I/O | Level | Description |
|---|---|---|---|---|
| 13 | USIM_DET | DI | 1.8V | SIM Detect |
| 14 | VREG_USIM | PO | 1.8V/2.85V | USIM Power |
| 15 | USIM_DATA | IO | 1.8V/2.85V | USIM Data |
| 16 | USIM_CLK | DO | 1.8V/2.85V | USIM Clock |
| 17 | USIM_RESET | DO | 1.8V/2.85V | USIM Reset |

### 3.8.1 USIM Reference circuit

CLM920_TE3 does not own USIM card slot, users need to design USIM card slot on their own interface board.
USIM interface as below：

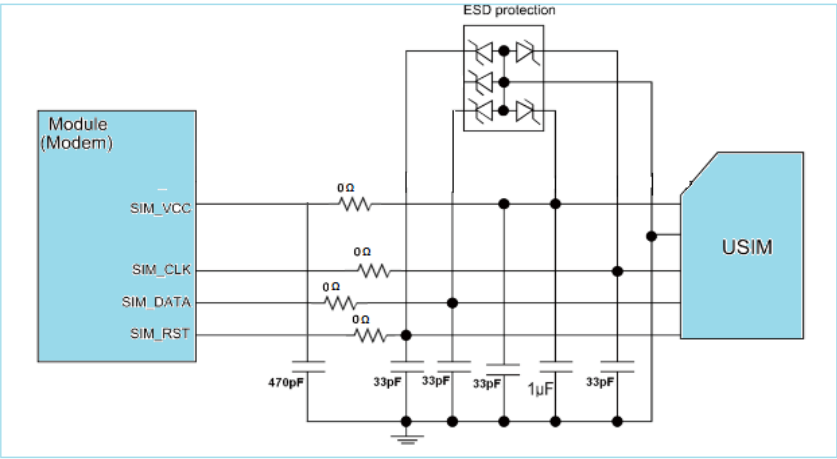



**Figure 11 USIM Reference circuit**

Design note：

- ✧ USIM interface reference design diagram is shown, the interface line should select the ESD protection device with a value less than 10 PF, and enhance the antistatic ability.
- ✧ USIM slot should be placed far away from the antenna RF radiation place
- ✧ SIM_DET pin detect "USIM" inserted or not. The default is high. When hot plug is used, the SIM card is detected by the PIN.

### 3.8.2 USIM_DET hot swap design

CLM920_TE3 4G support USIM hot swap function. The USIM_DET pin is used as an input detection pin to determine whether the SIM card is inserted or not. The USIM_DET pin defaults to a pull-up level.

Figure 3-10 hot swap

| NO | PIN | USIM_DET status | 描述 |
|---|---|---|---|
| 1 | 13 | HIGH | SIM inserted |
| 2 | 13 | LOW | SIM plug out |

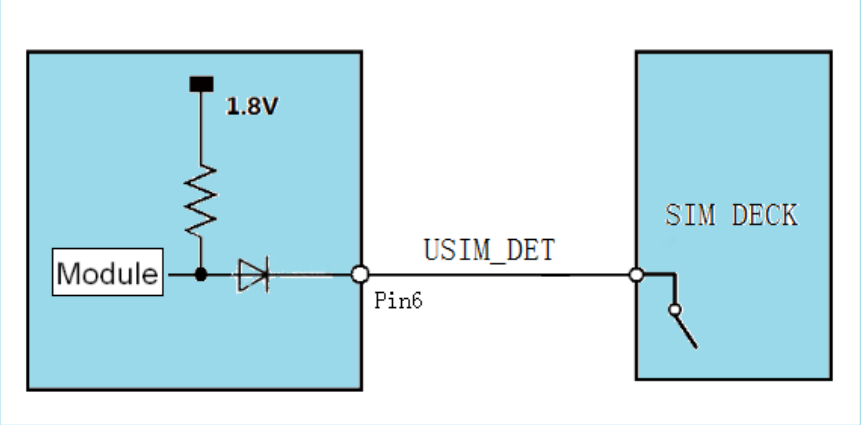



Figure **12 USIM detect circuit**

Use AT-command, user can ON/OFF this function. Reference AT command manual in details.

## 3.9 Airplane mode Interface

CLM920_TE3 4G provides W_DISABLE to turn ON/OFF RF function. In addition, the RF function can also be enabled or disabled by AT command. W_DISABLE function as below：

Figure 3-11 W_DISABLE Pin description

| NO | PINs | W_DISABLE Status | Function |
|---|---|---|---|
| 1 | 4 | H | Airplane mode ON |
| 2 | 4 | L | Airplane mode OFF |

Airplane mode reference design：

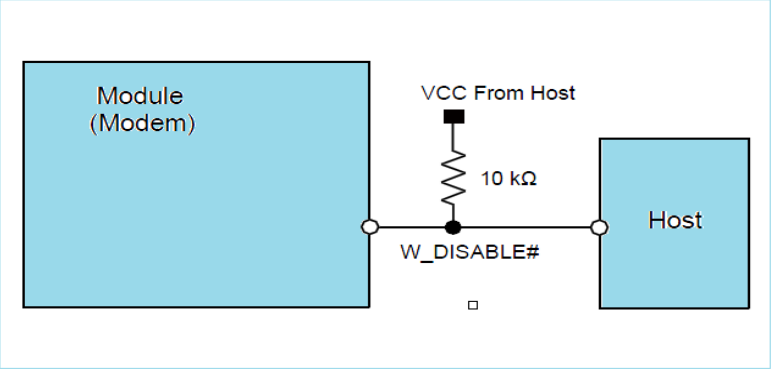



**Figure 12 Airplane mode reference design**

## 3.10 PCM and I2C Interface：

Module provides PCM and I2C interface, PCM mode：PCM Master, 2M clock, 8k sample rate,16 bit linear. PCM voice level is 1.8V, slave should be paid to level matching in application .

Only support PCM master.

Figure 3-12 PCM Pin definition

| PIN | Name | I/O | Level | Description |
|---|---|---|---|---|
| 24 | PCM_IN | DI | 1.8V | PCM IN |
| 25 | PCM_OUT | PO | 1.8V | PCM OUT |
| 26 | PCM_SYNC | IO | 1.8V | PCM SYNC |
| 27 | PCM_CLK | DO | 1.8V | PCM Clock |
| 41 | I2C_SCL | OD | 1.8V | I2C Clock |
| 42 | I2C_SDA | OD | 1.8V | I2C Data |
| 55 | MCLK | DO | 1.8V | Master Clock |

The following is a reference design of the PCM interface with an external codec chip ：

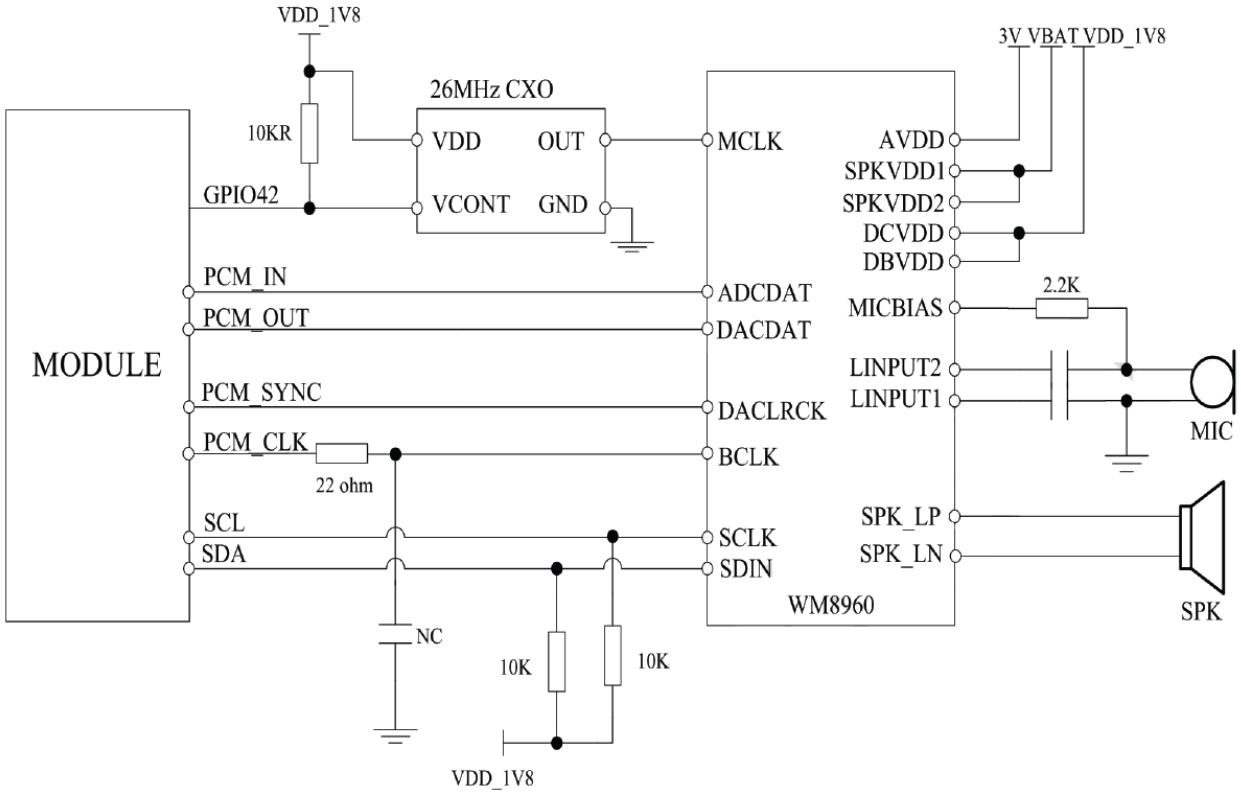



Figure **13** **PCM reference design**

## 3.11 SD Card

The module provides SD card interface, SDC2 is the SD card interface 1.8V/2.95V level, cannot be used as GPIO, only for SD card. Since the VREG_2.85V power supply can only provide the maximum 50mA current, the SD card power supply needs to be separately supplied with LDO to SD card power supply.

Figure 3-13 SD Pin description

| PIN | Name | I/O | Level | Description |
|---|---|---|---|---|
| 28 | SD_D3 | IO | 1.8V/2.85V | SDIO Data |
| 29 | SD_CLK | IO | 1.8V/2.85V | SDIO Clock |
| 30 | SD_CMD | DO | 1.8V/2.85V | SDIO Command |
| 31 | SD_D1 | IO | 1.8V/2.85V | SDIO Data |
| 32 | SD_D2 | IO | 1.8V/2.85V | SDIO Data |
| 33 | SD_D0 | IO | 1.8V/2.85V | SDIO Data |
| 34 | SD_INT | DI | 1.8V/2.85V | SD detect |
| 23 | VREG_2.85V | VDD | 2.85V | SD Power |

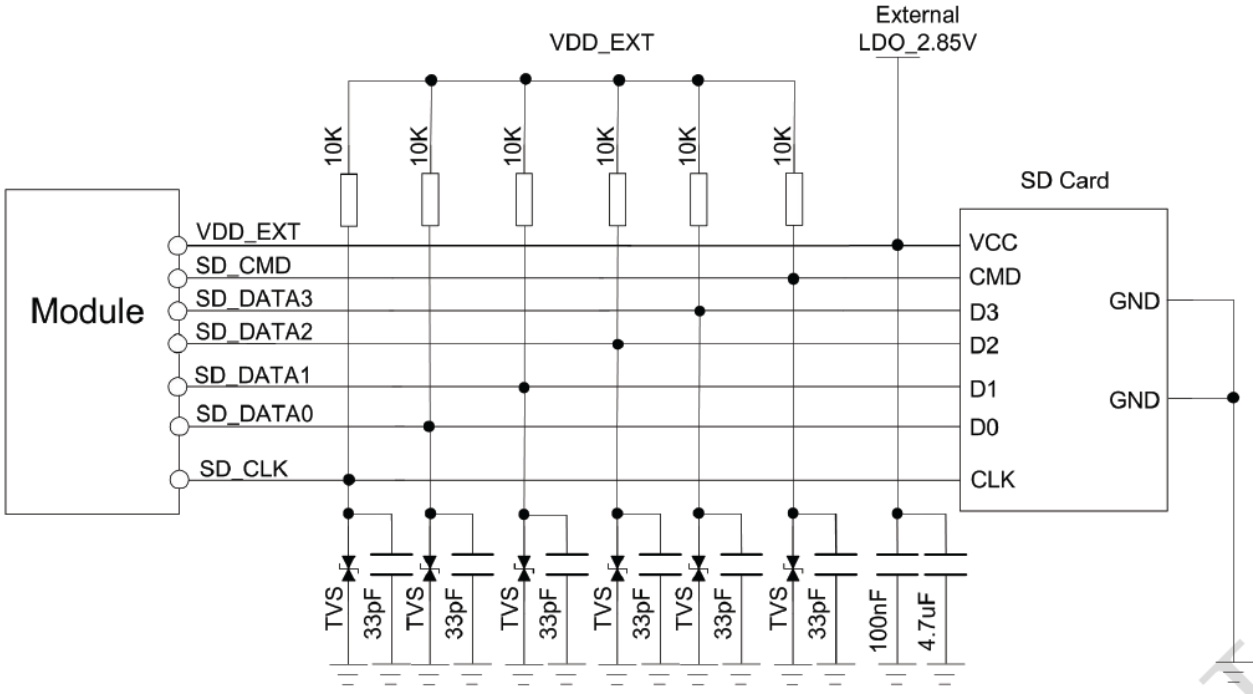



Figure **14** **SD reference design**

## 3.12 SPI Interface

CLM920_TE3 provides SPI interface. SPI voltage level is 1.8V, clock rate 26MHz.

Figure 3-14 SPI Pin description

| PINs | Name | I/O | Level | Description |
|---|---|---|---|---|
| 37 | SPI_MISO | DI | 1.8V | SPI IN（Main）/Out（Slave） |
| 38 | SPI_CS | DO | 1.8V | SPI Chip Select |
| 39 | SPI_CLK | DO | 1.8V | SPI Clock |
| 40 | SPI_MOSI | DO | 1.8V | SPI Out（Main）/IN（Slave） |

## 3.13 GPIO Interface

Figure 3-15 GPIO Pin description

| PIN | Name | I/O | Level | Description |
|---|---|---|---|---|
| 1 | WAKEUP_IN | DI | 1.8V | Wake up module |
| 2 | AP_READY | DI | 1.8V | Detect sleep status |
| 4 | W_DISABLE | DI | 1.8V | Control Airplane mode |

## 3.14 Network status LEDs

CLM920_TE3 4G provides three GPIOs to display working status.

Figure 3-16 Network indication LED

| Name | PIN | I/O | Description |
|---|---|---|---|
| NET_MODE | 5 | DO | Network status |
| NET_ STATUS | 6 | DO | Network status |
| STATUS | 61 | DO | Module status |

Figure 3-17 Status LED

| Status | LED status |
|---|---|
| Searching Network | Slow blink（period of 3s） |
| Voice call or Data call | Quick blink（period of 3s） |
| Registration OK, idle state | Quick blink（period of 0.2s） |

LED reference circuit as below：

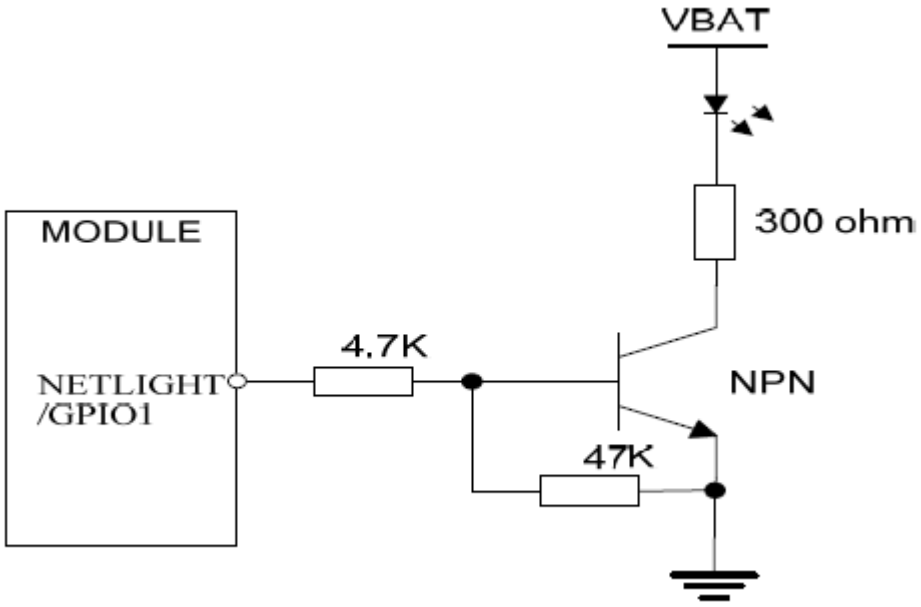



**Figure 15 reference design**

The brightness of the LED can be adjusted by adjusting the resistance value, maximum current can be adjusted to 40mA .

## 3.15 ADC Function

The module provides 2 channel analog to digital conversion interface, in order to make the ADC measurement more accurate, ADC needs to be packaged in wiring.

Figure 3-18 ADC Pin description

| PINs | Name | I/O | Level | Description |
|---|---|---|---|---|
| 44 | ADC1 | I | 0.3-VBAT | Analog input |
| 45 | ADC0 | I | 0.3-VBAT | Analog input |

# 4 Overall technical index

## 4.1 Overview of this chapter

CLM920_TE3 RF contains the following parts：

- ✧ Working frequency；
- ✧ Conducting RF measurement ；
- ✧ The receiving sensitivity and power conduction. ；

## 4.2 working frequency

Figure 4-1 working frequency

| Band | UL | DL | Duplex Mode |
|---|---|---|---|
| LTE B1 | 1920MHz– 1980MHz | 2110MHz – 2170MHz | FDD |
| LTE B3 | 1710MHz– 1785MHz | 1805MHz – 1880MHz | FDD |
| LTE B5 | 824MHz – 849MHz | 869MHz – 894MHz | FDD |
| LTE B38 | 2570MHz– 2620MHz | 2570MHz – 2620MHz | TDD |
| LTE B39 | 1880MHz– 1920MHz | 1880MHz – 1920MHz | TDD |
| LTE B40 | 2300MHz– 2400MHz | 2300MHz – 2400MHz | TDD |
| LTE B41 | 2555MHz– 2655MHz | 2555MHz – 2655MHz | TDD |
| GSM850 | 824MHz – 849MHz | 869MHz – 894MHz | GSM |
| GSM900 | 880MHz – 915MHz | 925MHz – 960MHz | GSM |
| GSM1800 | 1710MHz– 1785MHz | 1805MHz – 1880MHz | GSM |
| UMTS B1 | 1920MHz –1980MHz | 2110MHz – 2170MHz | WCDMA |
| UMTS B3 | 1710MHz –1785MHz | 1805MHz – 1880MHz | WCDMA |
| TDS B34 | 2010MHz –2025MHz | 2010MHz – 2025MHz | TD-SCDMA |
| TDS B39 | 1880MHz –1920MHz | 1880MHz – 1920MHz | TD-SCDMA |
| BC0 | 824MHz – 849MHz | 869MHz – 894MHz | CDMA |
| GPS | 1575.42MHz+/-1MHz | | |

## 4.3 Conduction radio frequency measurement

### 4.3.1 testing environment

Figure 4-2 Test instrument

| | |
|---|---|
| **Instrument** | R&S CMW500 |
| **Power supply** | Agilent 66319 |
| **RF cable** | Rosenberger Precision Microwave Cable |
| **Murata coaxial RF line** | MXHP32HP1000 |

### 4.3.2 Test standard

CLM920_TE3 follows 3GPP TS 51.010-1, 3GPP TS 34.121-1, 3GPP TS 36.521-1, 3GPP2 C.S0011 and 3GPP2 C.S0033 test standard. Each module is strictly tested in the factory to ensure the quality is reliable.

## 4.4 Sensitivity and transmitting power.

CLM920_TE3, sensitivity and transmit power test indicators are as follows ：

Figure 4-3 RF index

| Mode | Uplink | Downlink | Power | Sensitivity |
|---|---|---|---|---|
| GSM | 824~849MHz | 869~894MHz | 33±2dBm | <-108dBm |
| | 880~915MHz | 925~960MHz | 33±2dBm | <-108dBm |
| | 1710~1785MHz | 1805~1880MHz | 30±2dBm | <-108dBm |
| WCDMA | 1710~1785MHz | 1805~1880MHz | 23+2/-2dBm | <-109dBm |
| TD-SCDMA | 2010~2025MHz | 2010~2025MHz | 24+1/-3dBm | <-108dBm |
| | 1880~1920MHz | 1880~1920MHz | 24+1/-3dBm | <-108dBm |
| 1XEVDOrA | 824~849MHz | 869~894MHz | 23+2/-2dBm | <-108dBm |

CLM920_TE3, sensitivity and TX power test indicators are as follows：

Figure 4-4 4GRF sensitivity index

| Name | 3GPP standard | Rx sensitivity | | |
|---|---|---|---|---|
| | | MIN | Std. | MAX |
| LTE B1（FDD QPSK ）95%） | < –97(10 MHz) | | -98 | -97 |
| LTE B3（FDD QPSK ）95%） | < –94(10 MHz) | | -97 | -96 |
| LTE B5（FDD QPSK ）95%） | < –95(10 MHz) | | -97 | -96 |
| LTE B38（TDD QPSK ）95%） | < –97(10 MHz) | | -98 | -97 |
| LTE B39（TDD QPSK ）95%） | < –97(10 MHz) | | –98 | -97 |

| | | | | |
|---|---|---|---|---|
| LTE B40（TDD QPSK ）95%） | < –97(10 MHz) | | -98 | -97 |
| LTE B41（TDD QPSK ）95%） | < –97(10 MHz) | | -97 | -96 |

Figure 4-5 TX power index

| Name | 3GPP standard (dBm) | TX power | | |
|---|---|---|---|---|
| | | Min | Std | Max |
| LTE B1 | 21 to 25 | 22 | 23 | 24 |
| LTE B3 | 21 to 25 | 22 | 23 | 24 |
| LTE B5 | 21 to 25 | 22 | 23 | 24 |
| LTE B38 | 21 to 25 | 22 | 23 | 24 |
| LTE B39 | 21 to 25 | 22 | 23 | 24 |
| LTE B40 | 21 to 25 | 22 | 23 | 24 |
| LTE B41 | 21 to 25 | 22 | 23 | 24 |

## 4.5 Antenna Requirements

CLM920_TE3 antenna requirement as below:

Figure 4-6 antenna requirement

| Band | SWR | Gain (AVG) | Efficiency | TRP | TIS |
|---|---|---|---|---|---|
| GSM850 | <2.5:1 | 〉-4dbi | 〉40% | 29 | <-102 |
| GSM900 | | | | 29 | <-102 |
| GSM1800 | | | | 26 | <-102 |
| B1 FDD | | | | 19 | <-94 |
| B3 FDD | | | | 19 | <-91 |
| B38 TDD | | | | 19 | <-93 |
| B39 TDD | | | | 19 | <-93 |
| B40 TDD | | | | 19 | <-93 |
| B41 TDD | | | | 19 | <-93 |
| WCDMA B1 | | | | 19 | <-106 |
| CDMA BC0 | | | | 19 | <-106 |
| B34 TDS | | | | 19 | <-106 |
| B39 TDS | | | | 19 | <-106 |

CLM920_TE3, GNSS antenna requires an input impedance of 50 ohm, SWR< 2,
Passive antenna gain ： > 0dBi, Active antenna gain ： > -2dBi

## 4.6 Power consumption characteristics

Figure 4-7 GSM power consumption

| Band | Configure | PWR level | Current (mA) |
|---|---|---|---|
| GPRS850 | 1UP/1DL | 5 | 310 |

| | | | |
|---|---|---|---|
| GPRS900 | 1UP/1DL | 5 | 315 |
| GPRS1800 | 1UP/1DL | 0 | 200 |
| EDGE850 | 1UP/1DL | 8 | 220 |
| EDGE900 | 1UP/1DL | 8 | 225 |
| EDGE1800 | 1UP/1DL | 2 | 175 |

Figure 4-8 WCDMA power consumption

| Band | Power | Current (mA) |
|---|---|---|
| WCDMA B1 | 23.2dbm | 556 |
| | 1dbm | 165 |

Figure 4-9 LTE power consumption

| Band | Power dBm | Current (AVG） mA |
|---|---|---|
| B1 | 21.5 | 560 |
| B3 | 21.8 | 545 |
| B38 | 22.5 | 465 |
| B39 | 21.9 | 375 |
| B40 | 22.1 | 362 |
| B41 | 22.8 | 482 |

Figure 4-10 TDS-CDMA power consumption

| Band | Power dBm | Current（AVG）mA |
|---|---|---|
| TDS B34 | 22.8 | 173 |
| TDS B39 | 23.1 | 180 |

# 5 Antenna Interface

CLM920_TE3 provides three antenna, one is Main Antenna second is Diversity（Optional）and GNSS Antenna(optional). The connection with the antenna must be the line of 50 ohm characteristic impedance.

## 5.1 Main Antenna

CLM920_TE3 main Antenna need to obtain better RF performance, it is necessary to reserve PI matching circuit. In practical use, the device parameters can be matched according to board of the customers, and the 68~100nH inductor can be connected to the ground to prevent static electricity. Attention is paid to the impedance matching and antistatic or lightning stroke of the antenna .

Figure 5-1 Main Antenna Pin

| Name | PIN | I/O | Description |
|---|---|---|---|
| ANT_MAIN | 49 | IO | Main Antenna（50Ω ohm） |

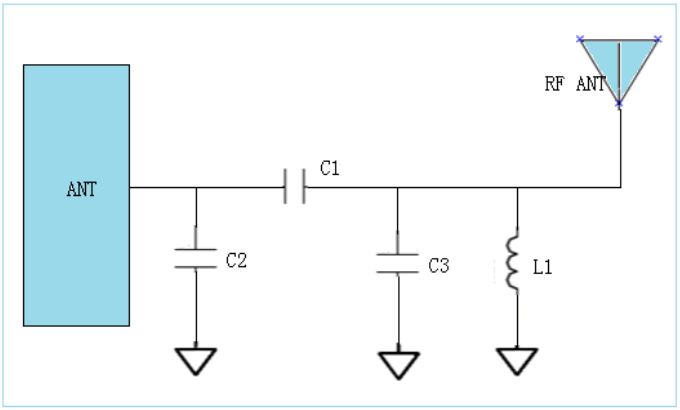



**Figure 16 Antenna interface**

## 5.2 Diversity Antenna interface

CLM920_TE3, Diversity antenna need to obtain better RF performance, it is necessary to reserve PI matching circuit. Parameters can be matched according to board of the customers, and the 68~100nH inductor can be connected to the ground to prevent static electricity. Attention is paid to the impedance matching and antistatic or lightning stroke of the antenna.

Figure 5-2 Diversity Pin definition

| Name | PIN | I/O | Description |
|---|---|---|---|
| ANT_DIV | 35 | AI | Diversity（50ΩOhm） |

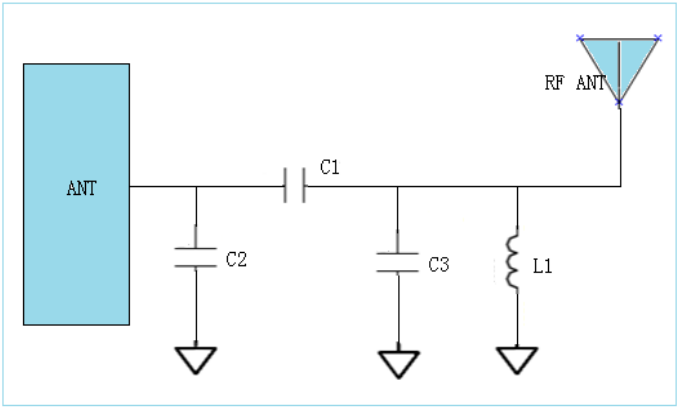



**图 17 Antenna interface**

## 5.3 GNSS Antenna

Support GPS, Beidou, GLONASS.

Figure 5-3 GNSS Antenna PIN

| Name | PIN | I/O | Description |
|---|---|---|---|

| | | | |
|---|---|---|---|
| ANT_GNSS | 47 | AI | GNSS Antenna（50Ω Ohm） |

Figure 5-4 GNSS RX frequency

| TYPE | Frequency |
|---|---|
| Beidou | 1561.098 ± 2.046MHz |
| GPS/Galileo/QZSS | 1575.42 ± 1.023MHz |
| GLONASS | 1597.5 ~ 1605.8MHz |

GNSS reference design can be designed according to the type of antenna, if a passive antenna is selected, design can add a PI type circuit just like the main diversity antenna and 100pF capacitor can be placed in the middle. For active antenna, it is necessary to supply the corresponding LDO to the antenna according to the type of active antenna after the series capacitor.

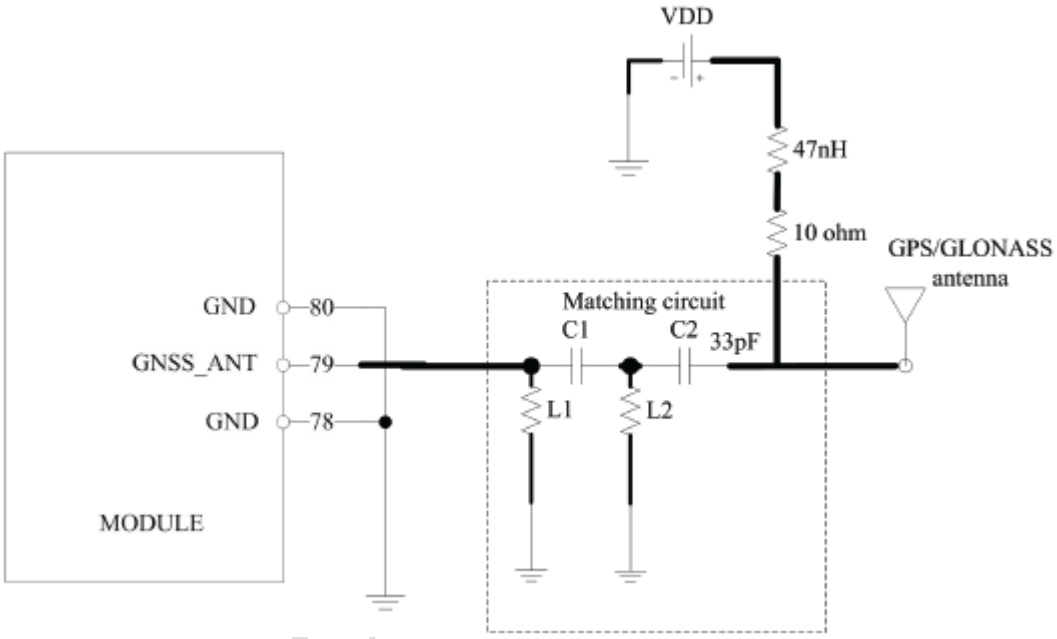



**图 18　GNSS 天线参考电路**

## 5.4 Antenna connector

CLM920_TE3, for a convenience antenna adjustment and authentication test, it is recommended that an antenna matching circuit and a radio frequency connector be added at the antenna interface of the module, RF connector recommended　HRS, U.FL-R-SMT-1(10)

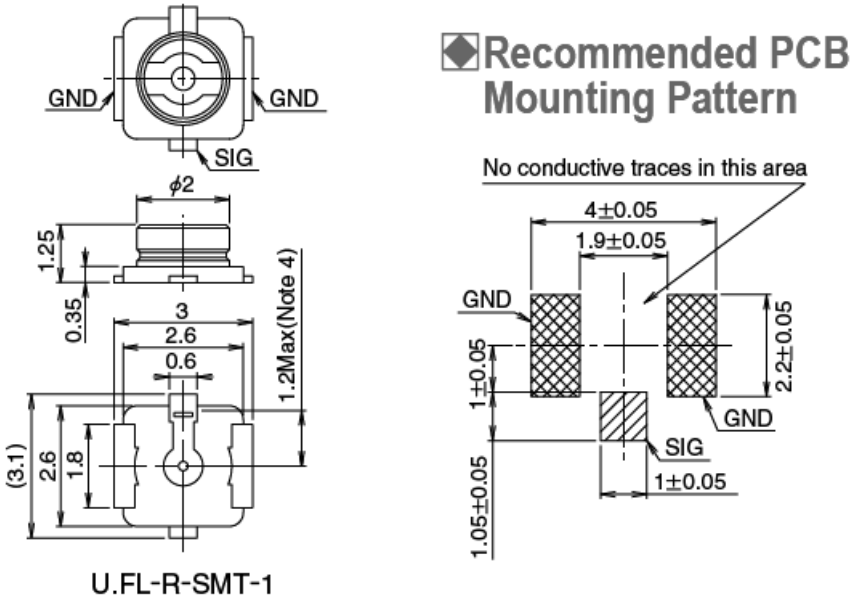



**Figure 19 Antenna connector**

RF connector plug fitted with this connector is HRS U.FL-LP series.

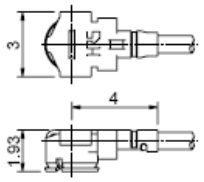
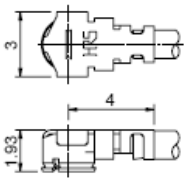
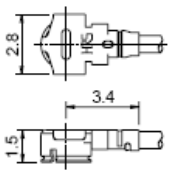
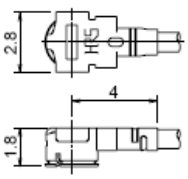
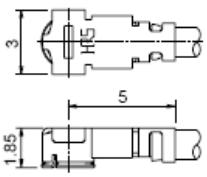
| Part No. | U.FL-LP-040 | U.FL-LP-066 | U.FL-LP(V)-040 | U.FL-LP-062 | U.FL-LP-088 |
|---|---|---|---|---|---|
| |  |  |  |  |  |
| Mated Height | 2.5mm Max. (2.4mm Nom.) | 2.5mm Max. (2.4mm Nom.) | 2.0mm Max. (1.9mm Nom.) | 2.4mm Max. (2.3mm Nom.) | 2.4mm Max. (2.3mm Nom.) |
| Applicable cable | Dia. 0.81mm Coaxial cable | Dia. 1.13mm and Dia. 1.32mm Coaxial cable | Dia. 0.81mm Coaxial cable | Dia. 1mm Coaxial cable | Dia. 1.37mm Coaxial cable |
| Weight (mg) | 53.7 | 59.1 | 34.8 | 45.5 | 71.7 |
| RoHS | YES | | | | |

**Figure 20 Antenna connector mating**

Mounting dimensions of connectors:

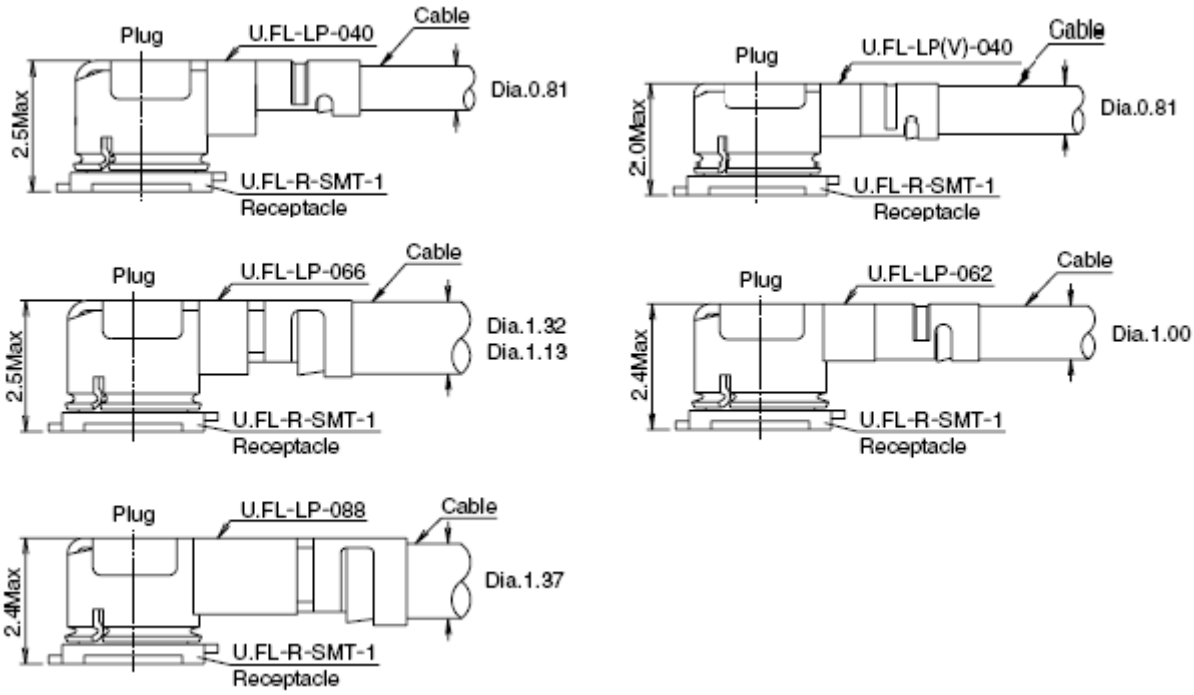



**Figure 21 Package size**

# 6 Interface electrical characteristics

## 6.1 Module I/O level

CLM920_TE3 I/O level as below：
For a 1.8V USIM use REG_USIM 1.8V and for a 3V USIM use REG_USIM 2.85V.
Other I/O voltage level is 1.8V.

Figure 6-1 CLM920_TE3 4G voltage level

| Parameter | Description | Minimum | Maximum |
|---|---|---|---|
| VIH | Voltage Input HIGH | 0.65*VDD_IO V | VDD_IO+0.3V |
| VIL | Voltage Input LOW | - | 0.35*VDD_IO V |
| VOH | Voltage Output HIGH | VDD_IO-0.45 V | VDD_IO V |
| VOL | Voltage Output LOW | 0V | 0.45V |

## 6.2 Electrostatic characteristics

CLM920_TE3, ESD protection is needed when the module is used.

Figure 6-2 CLM920_TE3 ESD test

| Test port | contact | Air discharge | Unit |
|---|---|---|---|
| USB | ±4 | ±8 | KV |
| USIM | ±4 | ±8 | KV |

| | | | |
|---|---|---|---|
| Analog Voice | ±4 | ±8 | KV |
| VBAT | ±4 | ±8 | KV |

# 7 Mechanical characteristics

## 7.1 appearance

CLM920_TE3, is a single sided PCB, appearance is shown below


**Figure 22 CLM920_TE3** appearance

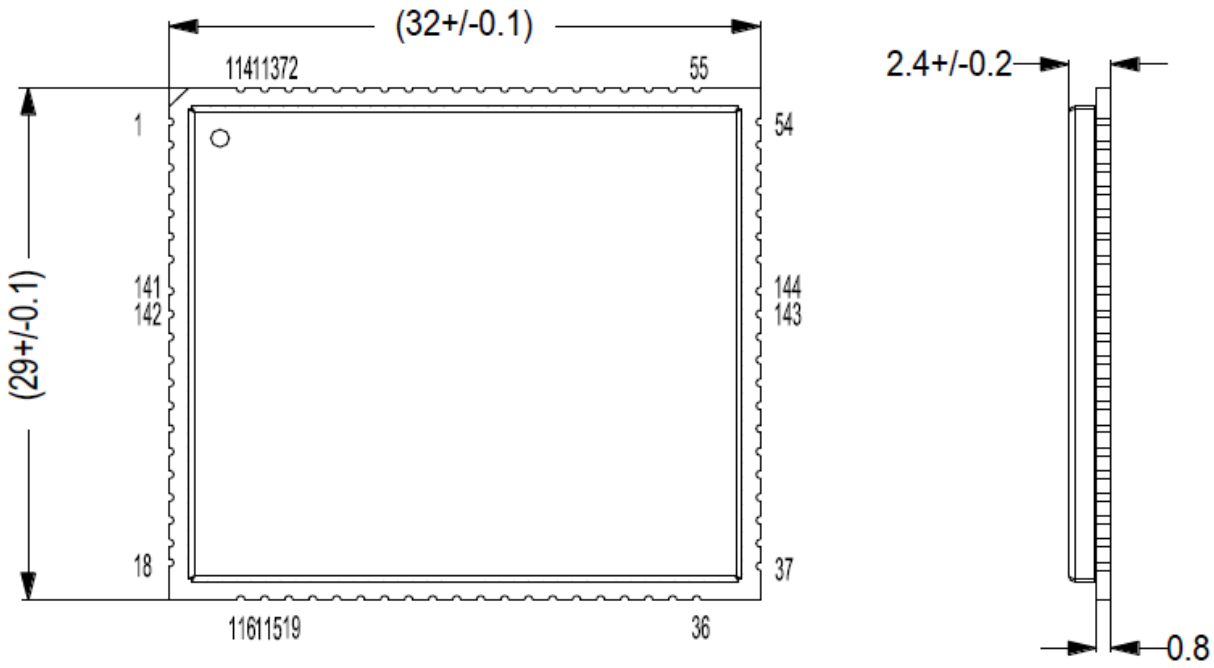



**Figure 23 CLM920_TE3 size**

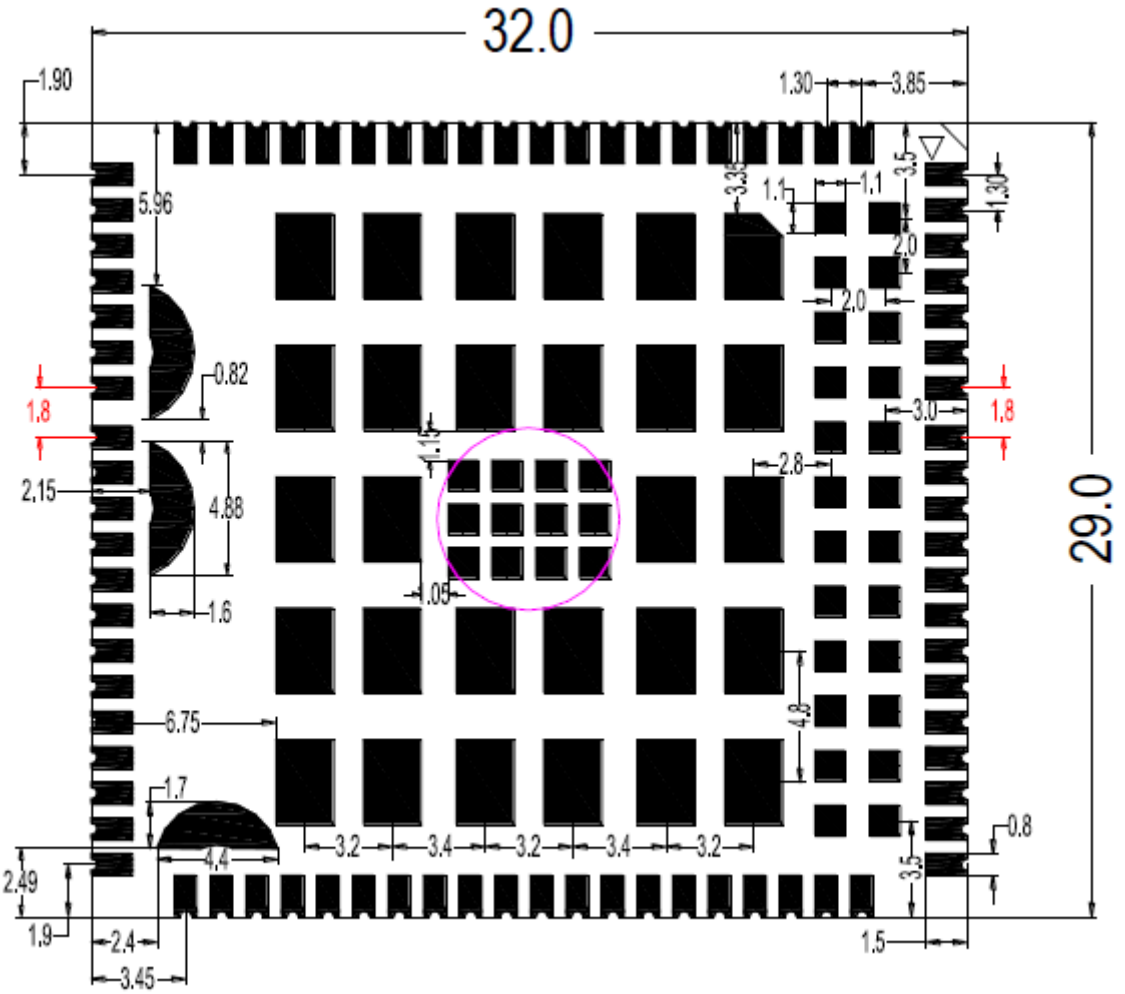



Figure **24 CLM920_TE3 Bottom View**

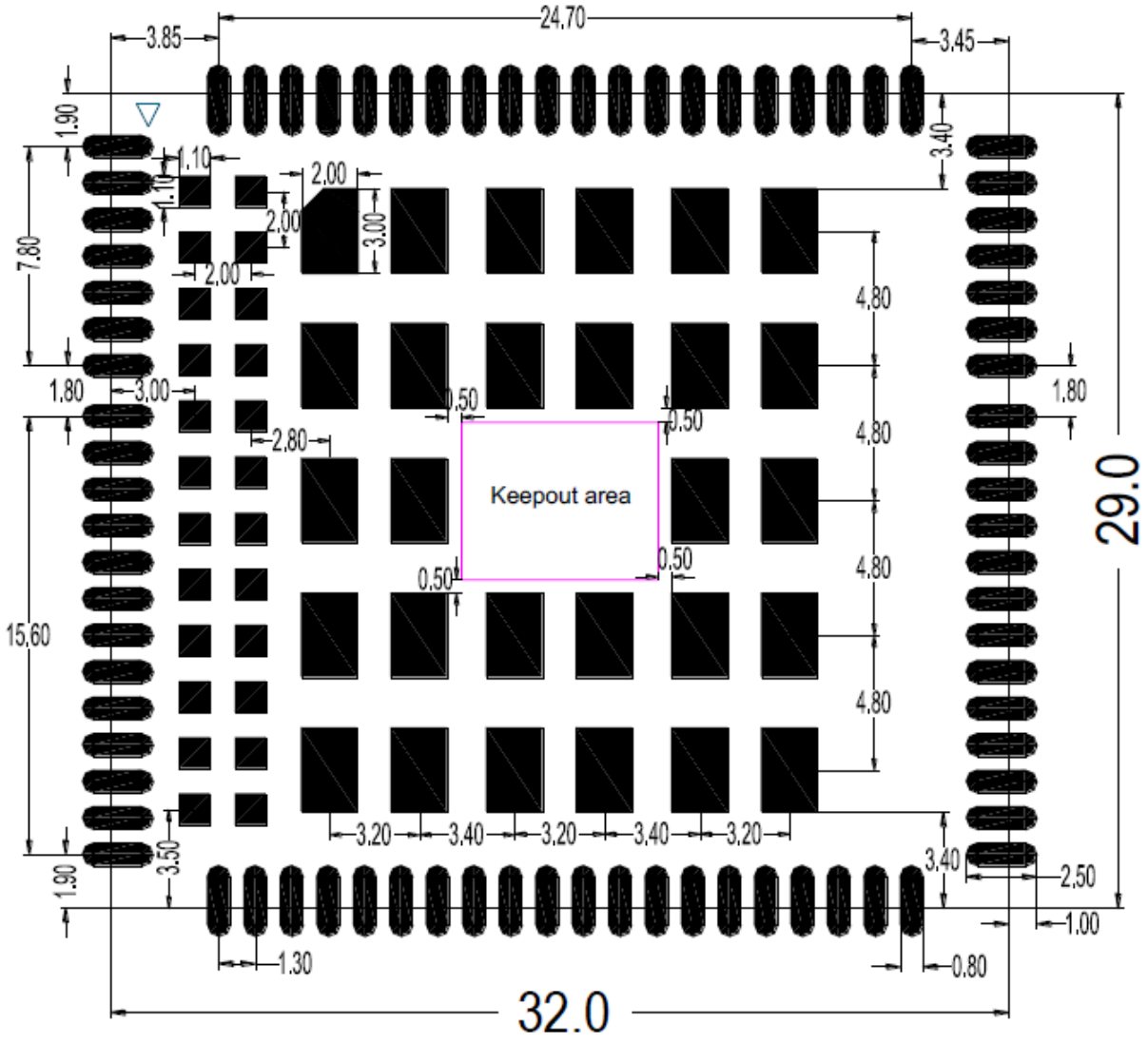



**Figure 25 CLM920_TE3 Package**

# 8 Typical reference design

# 9 Packaging and production

## 9.1 packaging and storage

CLM920_TE3, packaging with pallets, is sealed by vacuum sealing bag, 10pcs one pallet, one package contains 100pcs, shipped in the form of vacuum sealing bag. The storage of modules follows the following conditions ：

1. When the ambient temperature is below 40 degrees centigrade and the air humidity is less than 90%, the module can be stored in vacuum sealed bag for 12 months.

2. When the vacuum sealing bag is opened, the reflow soldering process or other high temperature process can be carried out directly if the following conditions are met:

- Storage air humidity is less than 10%.
- Environment temperature is less than 30 degrees Celsius, air humidity is less than 60%, the factory completes the patch within 72 hours.

3. If the module is in the following conditions, it is necessary to bake before the chip：

- When the ambient temperature is 23 degrees Celsius (allowing fluctuations of up and down 5 degrees Celsius), the humidity indicator card shows that the humidity is greater than 10%.

When the vacuum sealing bag is opened, the module environment temperature is less than 30 degrees Celsius, the air humidity is less than 60%, but the factory cannot complete the patch within 72 hours. When the vacuum sealing bag is opened, the module stores the air humidity greater than 10%.

4. If the module needs baking, remove the modules and bake for 48 hours at 125 degrees Celsius (allowing fluctuations of up to 5 degrees Celsius).

## 9.2 Production welding

The paste is printed on the halftone printing scraper, the solder paste stencil openings through the screen to PCB, squeegee efforts need to adjust the appropriate module to ensure the quality of solder paste, stencil thickness corresponding to the CLM920_TE3 module of the pad portion should be 0.18mm.

Recommended reflow temperature is 235~245 degrees C, cannot exceed 260 degrees C. In order to avoid repeated heat damage, it is recommended that the customer PCB board completes the reflow process and then paste the module.

The recommended furnace temperature curve is shown in the following picture.

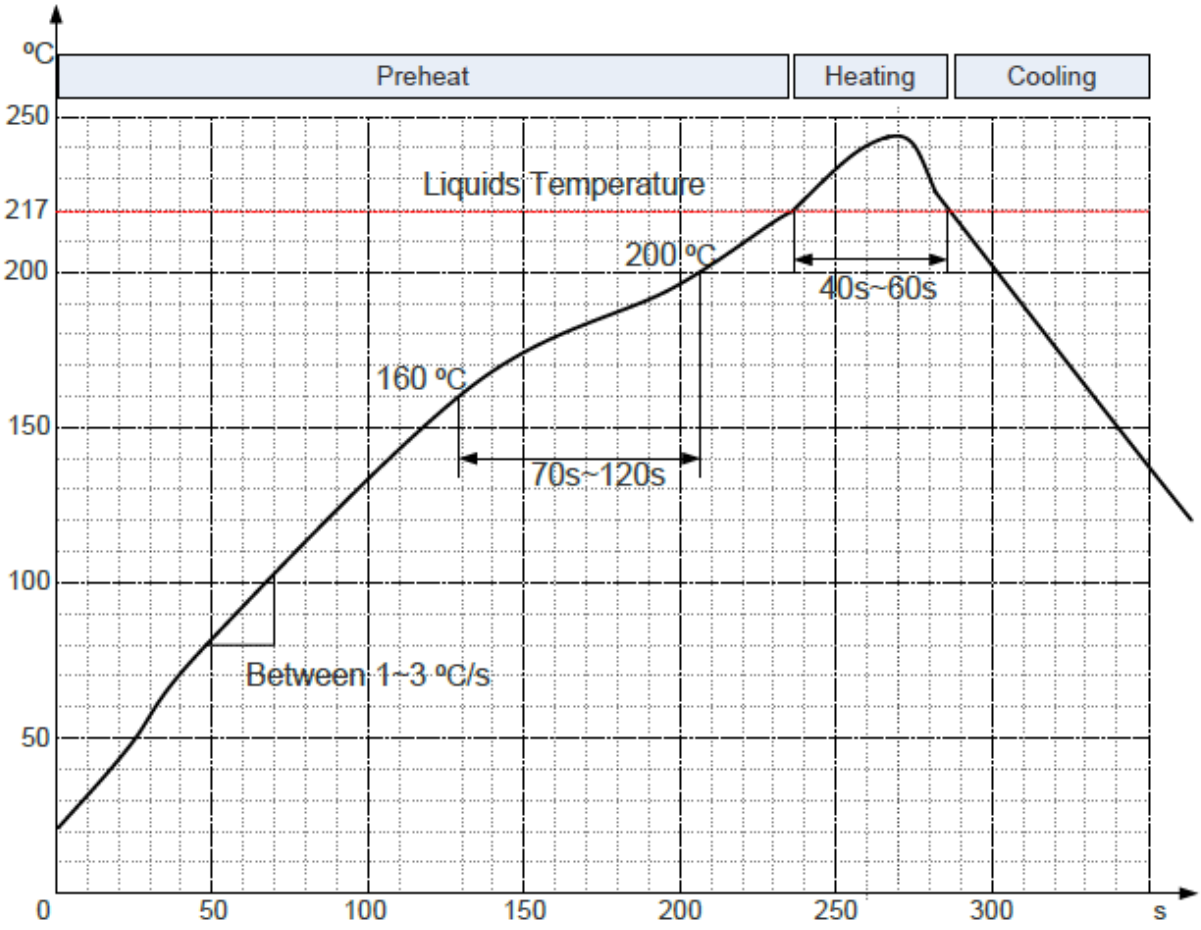



**Figure 26 Reflow soldering temperature diagram**